



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/777,620

02/11/2004

John Thomas Contreras

HSJ9-2003-0095US1

4619

(0107-0)

7590

05/02/2006

EXAMINER

NEGRON, DANIEL L

John J. Oskorep
One Magnificent Mile Center
Suite 1400
980 N. Michigan Avenue
Chicago, IL 60611

ART UNIT

PAPER NUMBER

2627

DATE MAILED: 05/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/777,620

Applicant(s)

CONTRERAS ET AL

Examiner

Daniell L. Negrón

Art Unit

2627

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11 February 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-30 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-8, 10-17 and 20-30 is/are rejected.
- 7) ☒ Claim(s) 9-11, 18 and 19 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 11 February 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on February 11, 2004 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement has been considered by the examiner.

Claim Objections

2. Claim 11 is objected to because of the following informalities: The limitation disclosed on lines 5-7 of claim 11 is repeated twice. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 2, 4, 6, 12, 14, 20, 22, and 26-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Gill U.S. Patent No. 5,825,595.

Regarding claim 1, Gill discloses a preamplifier circuit comprising a first input port configured to receive a first signal which includes a read sensor data signal and an interference signal (i.e., noise), a second input port configured to receive a second signal which includes the interference signal but not the read sensor data signal, and a subtractor (216) having first and second inputs coupled to the first and the second input ports respectively (Fig. 2, column 7, lines 27-31, and column 10, lines 23-31).

Regarding claim 2, Gill discloses a preamplifier circuit comprising an output (218) which provides the read sensor signal substantially without the interference signal (column 10, lines 23-31).

Regarding claim 4, Gill discloses a preamplifier circuit comprising a first bias source (208) which provides a first read sensor current/voltage bias at the first input port and a second bias source (210) which provides a second read sensor current voltage bias at the second input port (column 6, lines 5-12).

Regarding claim 6, Gill discloses a preamplifier circuit comprising a first amplifier (212) having an input coupled to the first input port and an output coupled to the first input of the subtractor (216), and a second amplifier (214) having an input coupled to the second input port and an output coupled to the second input of the subtractor (see Fig. 2 and disclosure thereof).

Regarding claims 12, 14, 20, 22, claims 12, 14, 20, 22 have limitations similar to those treated in the above rejections, and are met by the references as discussed above.

Regarding claims 26-30, method claims 26-30 are drawn to the method of using the corresponding apparatus claimed in claims 1, 2, 4, and 6. Therefore method claims 26-30 correspond to apparatus claims 1, 2, 4, and 6 and are rejected for the same reasons of anticipation as used above.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

Art Unit: 2627

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 3 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gill U.S. Patent No. 5,825,595 in view of Hedberg et al U.S. Patent No. 4,577,240.

Regarding claims 3 and 21, Gill discloses a preamplifier circuit comprising all the limitations of claims 1 and 20 as discussed above but fails to explicitly show the preamplifier embodied on an integrated circuit.

However, Hedberg et al disclose a preamplifier circuit embodied on an integrated circuit for the purpose of reducing the size of the circuit (column 26, line 39 through column 27, line 13).

Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to embody the preamplifier circuit disclosed by Gill on an integrated circuit as shown by Hedberg et al since doing so would allow the preamplifier to be a reduced size and to occupy less space.

7. Claims 5, 7, 8, 13, 15-17 and 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gill U.S. Patent No. 5,825,595 in view of Jove et al U.S. Patent No. 5,523,898.

Regarding claims 5, 7, and 8, claims, 5, 7, and 8, disclose limitations similar to those treated in the above rejections of claims 1, 2, 4, and 6. Furthermore, Gill discloses a preamplifier circuit comprising all the limitations of claim 1 as discussed above including a first read sensor current/voltage bias at the first input port and a second bias source (210) which provides a second read sensor current voltage bias at the second input port (column 6, lines 5-12), a first amplifier (212) having an input coupled to the first input port and an output coupled to the first

Art Unit: 2627

input of the subtractor (216), and a second amplifier (214) having an input coupled to the second input port and an output coupled to the second input of the subtractor (see Fig. 2 and disclosure thereof), but fails to explicitly show the second read sensor bias set to zero or being negligible.

Jove et al disclose a preamplifier wherein the bias current value is reduced to a negligible value during a write operation for the purpose of improving magnetic stability in a read circuit (see Abstract, column 1, lines 23-32, and lines 53-60).

Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the preamplifier circuit disclosed by Gill with the disclosure of reducing bias current of Jove et al in order to avoid magnetic instability and to lower power consumption of the circuit.

Finally, Gill and Jove et al fail to disclose a preamplifier circuit wherein a gain of at least one of the first and the second amplifiers is controllably adjusted so that an output of the subtractor provides the read sensor signal substantially without the interference signal however, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide adjustable gain amplifiers, since it has been held that the provision of adjustability, where needed, involves only routine skill in the art. *In re Stevens*, 101 USPQ 284 (CCPA 1954).

Regarding claims 13, 15-17 and 23-25, claims 13, 15-17 and 23-25 have limitations similar to those treated in the above rejections, and are met by the references as discussed above.

Allowable Subject Matter

8. Claims 9-11, 18, and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claims 9 and 18, prior art fails to disclose a preamplifier comprising the limitations of claims 1 and 12, further comprising a first amplifier which includes a first transistor having a base coupled to the first input port, a collector coupled to a first reference voltage through a first resistor, and an emitter coupled to a second reference voltage, and a second amplifier which includes a second transistor having a base coupled to the second input port, a collector coupled to the first reference voltage through a second resistor, and an emitter coupled to the second reference voltage.

Regarding claims 10, 11, and 19, prior art fails to disclose a preamplifier comprising the limitations of claims 1 and 12 further comprising a first amplifier which includes a first transducer having a base coupled to a first input port through a first capacitor, a collector coupled to a first reference voltage through a first resistor, and an emitter coupled through a second reference voltage, and a second amplifier which includes a second transistor having a base coupled to the second input port through a second capacitor, a collector coupled to the first reference voltage through a second resistor, and an emitter coupled to the second reference voltage.

Art Unit: 2627

Conclusion

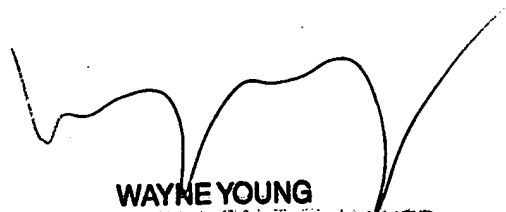
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniell L. Negrón whose telephone number is 571-272-7559. The examiner can normally be reached on Monday-Friday (8:30am-5:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wayne R. Young can be reached on 571-272-7582. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


DLN

April 18, 2006


WAYNE YOUNG
SUPERVISORY PATENT EXAMINER